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EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2189	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/735,266	Applicant(s) GODFREY, KEVIN P.	
	Examiner Kim T. Huynh	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6-13, 15-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Stewart et al. (US Patent 5,557,764)

a. As per claim 1, Steward discloses in a system comprising a processor configured to execute program code instructions stored in a program store, a pre-stored vector interrupt handling system, comprising:

- an interrupt vector store comprising a plurality of interrupt vectors; (abstract, col.2, lines 6-14)
- an interrupt control device connected to a plurality of interrupt request signals, said interrupt control device outputting an interrupt request signal to the processor; and (col.2, lines 6-14)
- a selector, responsive to the processor's cycle type signal, for selecting between a program code instruction from the program store and an interrupt vector from said interrupt vector store to be loaded into an execution unit of the processor. (col.2, lines 6-17)

b. As per claim 2, Stewart discloses the interrupt control device includes a prioritizer for prioritizing the plurality of interrupt request signals. (col.5, lines 5-16)

c. As per claim 3, Steward discloses the prioritizer asserts an interrupt identifier signal to the interrupt vector store for identifying which interrupt vector to load into said execution unit. (col.7, lines 35-48)

d. As per claim 6, Stewart discloses the interrupt vector store is pre-programmed with interrupt vectors, each of said interrupt vectors being a branch instruction that jumps to an interrupt service routing in the program store. (col.2, lines 21-40)

e. As per claim 7, Stewart discloses the interrupt vector store is implemented in read-only memory (ROM). (fig.2, 26), (col.5, lines 38-42)

f. As per claim 8, Stewart discloses the interrupt sources include one or more of data input devices, data output devices, embedded hardware devices, and data storage devices. (col.6, lines 9-10)

g. As per claim 9, Stewart discloses the pre-stored vector interrupt handling system is incorporated in a computer system. (col.2, lines 6-17)

h. As per claim 10, Stewart discloses the pre-stored vector interrupt handling system is incorporated in a microcontroller. (fig.1, 60)

i. As per claim 11, Stewart discloses the processor is a microprocessor. (fig.1, 60)

j. As per claim 12, Stewart discloses the microprocessor includes a cache. (fig.2, 24)

k. As per claim 13, Stewart discloses the microprocessor includes a means for pre-fetching instructions. (abstract, col.5, lines 47-52)

l. As per claim 15, Stewart discloses system further comprising a multiplexer for selecting between an initialization mode and an interrupt mode. (abstract, col.6, lines 6-7, 26-27), wherein selected mode can be various)

m. As per claim 16, Stewart discloses the selector is connected to a cycle type output signal from the processor. (col.2, lines 21-40)

n. As per claim 17, Steward discloses the selector asserts a chip select control signal to the interrupt vector store and de-asserts a chip select control signal to the program store if the cycle type output signal from the processor is an interrupt cycle, (col.3, lines 36-42) and de-asserts said control signal to the interrupt vector store and asserts said chip select signal to the program store if the cycle type output signal from the processor is a non-interrupt instruction cycle. (col.4, lines 21-28), (col.5, lines 6-21), (col.6,lines 4-25), wherein signals activate when assert (trigger) vice versa, (col.3, lines 21-48), wherein vectors(fig.2, 10, 11, 13, 15, 17 etc) to program store, and vectors in slot memory (fig.2, 32 interrupt vectors)

p. As per claim 18, Steward discloses the selector is connected to a read/write output signal from the processor, (col.4, lines 24-25), which read/write output signal is used by the selector to place the interrupt vector store into a read mode if the cycle type output signal from the processor is an interrupt cycle. (fig.2, 60), (col.2, lines 6-17) (col.3, lines 21-48), wherein vectors(fig.2, 10, 11, 13, 15, 17 etc) to program store, and vectors in slot memory (fig.2, 32 interrupt vectors)

q. As per claim 19, Stewart discloses the processor is a digital signal processor (DSP) (fig.1, 60)

r. As per claim 20, Stewart discloses in a system comprising a processor, a method for pre-stored vector interrupt handling, comprising the steps of:

- intercepting a processor's normal instruction fetch bus cycle; (fig.2, 16), (col.3, lines 21-22)
- generating an interrupt identifier signal to the interrupt vector store; (col.2, lines 6-17)
- delivering a pre-stored interrupt vector directly to the execution unit of the processor, said pre-stored interrupt vector dependent upon said interrupt identifier signal. (col.2, lines 6-17), abstract)

s. As per claim 21, Stewart discloses the method further comprising the step of initializing the interrupt vector store. (fig.4, 132), (col.3, lines 21-26)

t. As per claim 22, Stewart discloses the step of initializing the vector store further comprises the step of pre-storing the interrupt vector store with a plurality of interrupt vectors. ((fig.4, 132), abstract, col.2, lines 6-17)

u. As per claim 23, Steward discloses the processor's normal instruction fetch bus cycle further comprises the step of ensuring that the interrupt vector store has exclusive control of the data bus by asserting a chip select control signal to the interrupt vector store and de-asserting a chip select control signal to the program store. (col.3, lines 21-48), wherein vectors(fig.2, 10, 11, 13, 15, 17 etc) to program store, and vectors in slot memory (fig.2, 32 interrupt vectors)

v. As per claim 24, Stewart discloses a system for handling interrupts in a processor-controlled device, said processor-controlled device comprising a processor executing a software program stored as a set of program instructions, the system comprising:

- an interrupt vector store; (fig.2, 32), abstract)
- an interrupt controller connected a plurality of interrupt request signals, said interrupt controller outputting a master interrupt signal; and (col.2, lines 6-14)
- a selector in a controlling arrangement with said interrupt vector store and with a memory storing program instructions being executed by the processor, said selector causing the processor to receive the next program instruction when the master interrupt signal is not asserted, and to receive an interrupt vector (branch instruction op-code and address) from the interrupt vector store when the master interrupt signal is asserted. (col.2, lines 6-17)

w. As per claim 25, Stewart discloses interrupt vector is provided directly to an execution unit of the processor. (fig.2, 20), abstract)

x. As per claim 26, Stewart discloses interrupt vector store is dynamically loaded with one or more interrupt vectors when the processor is running. (col.5, lines 53-65), (col.3, lines 22-26)

y. As per claim 27, Stewart discloses interrupt vector store is statically pre-loaded with one or more interrupt vectors. (fig.4, 132), abstract)

z. As per claim 28, Stewart discloses processor is connected to a system bus, and wherein said selector causes the processor to receive the next program instruction by asserting a first select signal connected to said memory storing said program instructions when the master interrupt signal is nt asserted, and causes the processor to receive said interrupt vector from the interrupt vector store by asserting a second select signal connected to said interrupt vector store when the master interrupt signal is asserted. (col.2, lines 6-17)

a1. As per claim 29, Stewart discloses interrupt vector store comprises a plurality of interrupt vectors, each interrupt vector corresponding to a different interrupt request signal. (col.2, lines 6-17)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stewart et al. (US Patent 5,557,764) in view of Fudeyasu et al. (US Patent 6,154,837)

Steward discloses all the limitations as above except the interrupt control device comprises a register masking the plurality of interrupt request signals. However, Fudeyasu discloses the RAM store maskable interrupt vectors. (col.2, lines 31-33)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Fudeyasu's teaching into Steward's method to have

a register for maskable vectors so as to filter out the maskable and for distinguish difference mode of system, either maskable for erasable or unmaskable for transferable. (col.2, lines 31-46)

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stewart et al. (US Patent 5,557,764) in view of Christie (Pub. No. 20020019902)

Steward discloses all of the limitations as above except system is included in a wireless communication device. However Christie discloses receiving, sending or storing instructions data implemented in accordance with the foregoing description upon a carrier medium which may include transmission media conveyed via a wireless link.[0077]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Christie's teaching into Steward's method to have a wireless communication system so as to be convenience, saving space, no complex wires and as to be compatible with latest advancements in the computer system.

Conclusion

6. *A shortened statutory period for reply is set to expire THREE months from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) months from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) months from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C 133).*

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

May 28, 2003

RUPAL DHARIA
PRIMARY EXAMINER